CLAIMS

WE CLAIM:

1. A method for generating a layout, comprising the steps of:

applying a 2-layer geometry-operation algorithm to a first layout and a second layout, wherein the first layout is not resolution-enhanced and the second layout is a resolution-enhanced version of the first layout; and

generating a third layout, wherein the third layout comprises one or more fragments, the one or more fragments comprising one or more biases, the one or more biases according to one or more amounts of resolution-enhancement of the second layout as compared to the first layout.

2. A data structure for representing an intermediate resolution-enhancement state layout fragment, the data structure indicating a location of the fragment and a bias of the fragment.

3. The data structure of claim 2, further indicating a type of the fragment.

4. A method for performing resolution-enhancement, comprising the steps of:

assembling a plurality of layouts into a full-chip assembly, a first layout of the plurality of layouts comprising an intermediate resolution-enhancement state layout; and

verifying the full-chip assembly.

5. The method of Claim 4, further comprising generating a result of the verifying step, the result comprising a simulation-based verification result or a geometry-based verification result, the result for serving as input into a damping algorithm, the damping algorithm for re-converging a resolution-enhancement of the first layout.

6. The method of Claim 4, further comprising the steps of:

selecting a first layout fragment of the first layout; and

adjusting a resolution-enhancement of the first layout fragment, the adjusting step according to a result of the verifying step.

7. The method of Claim 6, wherein the result of the verifying step comprises a simulation-based verification result or a geometry-based verification result.

8. A method for performing resolution-enhancement, comprising the steps of:

modifying a first layout in a full-chip layout assembly to produce a second modified layout;

converting the second modified layout to a third intermediate resolution-enhancement state layout;

inserting the third intermediate resolution-enhancement state layout into the full-chip assembly for verification;

wherein the modifying step comprises a re-design of an IP block, IP core or library within the first layout according to an engineering change order.

9. The method of Claim 8, further comprising the step of verifying the full-chip assembly.

10. A method for locally perturbing layout resolution-enhancement, comprising the steps of:

determining an interacting neighborhood of a layout fragment, the layout fragment comprising a fragment resolution-enhancement, the interacting neighborhood comprising a halo extended from the layout fragment according to a proximity range of a manufacturing process;

assigning a damping factor to the layout fragment, the damping factor according to a proximity of the layout fragment to a center of the interacting neighborhood; and

adjusting the fragment resolution-enhancement according to the damping factor.

11. An engineering workstation, comprising:

a processor; and

a memory unit;

wherein the memory unit comprises instructions for (a) assembling a plurality of layouts into a full-chip assembly, a first layout of the plurality of layouts comprising an intermediate resolution-enhancement state layout, and (b) verifying the full-chip assembly.

12. A data structure for representing a plurality of attributes, the plurality of attributes describing a plurality of intermediate resolution-enhancement state layout fragments, the

plurality of attributes comprising one or more fragment locations, one or more fragment types and one or more fragment biases, wherein a first one or more attributes of the plurality of attributes are grouped according to a proximity of a first one or more fragments of the plurality of fragments.

13. A method for performing resolution-enhancement, comprising the steps of:

selecting a first plurality of layout blocks in a layout;

generating (a) a first block comprising a set of layout elements common to the first plurality of layout blocks, and (b) a plurality of difference-sets representing differences between (1) layout blocks in the first plurality of layout blocks and (2) the first block; and

performing resolution-enhancement on the first block to obtain a second resolution-enhanced block;

wherein the first and second blocks are in intermediate resolution-enhancement state.

14. The method of Claim 13, further comprising the steps of:

combining the plurality of difference-sets with the second resolution-enhanced block to obtain a second plurality of resolution-enhanced blocks; and

inserting the second plurality of resolution-enhanced blocks into the layout.

15. The method of Claim 14, further comprising the step of re-converging one or more boundaries of the second plurality of resolution-enhanced blocks, wherein the re-

converging step proceeds according to a set of neighbors of the second plurality of resolution-enhanced blocks.

16. A method for performing resolution-enhancement, comprising the steps of:

performing a first resolution-enhancement on a layout;

modifying a first block of the layout, wherein the first block is in intermediate resolution-enhancement state;

performing a second resolution-enhancement on the first modified block; and

re-converging a resolution-enhancement of the first modified block according to a damping algorithm and according to a set of neighbors of the first modified block.

17. The method of Claim 16, further comprising the step of verifying the layout after the re-converging step.

18. The method of Claim 16, wherein the performing a second resolution-enhancement step comprises mirroring the first modified block to simulate a set of neighbors around the first modified block.

19. A method for performing resolution-enhancement, comprising the steps of:

performing a first resolution-enhancement on a first circuit block and a second resolution-enhancement on a second circuit block;

assembling the first and second resolution-enhanced circuit blocks to obtain a third aggregate circuit block; and

re-converging a resolution-enhancement of the third aggregate circuit block according to a damping algorithm;

wherein the first and second circuit blocks and the third aggregate circuit block are in intermediate resolution-enhancement state.

20. The method of Claim 19, wherein the performing step comprises mirroring the first circuit block to simulate a set of neighbors around the first circuit block.

21. A method for performing resolution-enhancement, comprising the steps of:

assembling a plurality of resolution-enhanced layouts to obtain a first aggregate layout;

verifying the first aggregate layout to obtain a verification result;

modifying a first circuit block of the plurality of resolution-enhanced layouts according to the verification result to obtain a second modified aggregate layout, wherein the first circuit block is in intermediate resolution-enhancement state; and

re-converging a resolution-enhancement of the first circuit block according to a damping algorithm and according to a set of neighbors of the first circuit block.

22. The method of Claim 21, further comprising the step of re-verifying the second aggregate layout.

23. A method for performing resolution-enhancement, comprising the steps of:

obtaining (a) a layout in intermediate resolution-enhancement state, the layout comprising a resolution-enhancement according to a first set of resolution-enhancement parameters, and (b) a second set of resolution-enhancement parameters;

re-converging a resolution-enhancement of the layout according to the second set of resolution-enhancement parameters and according to a damping algorithm.